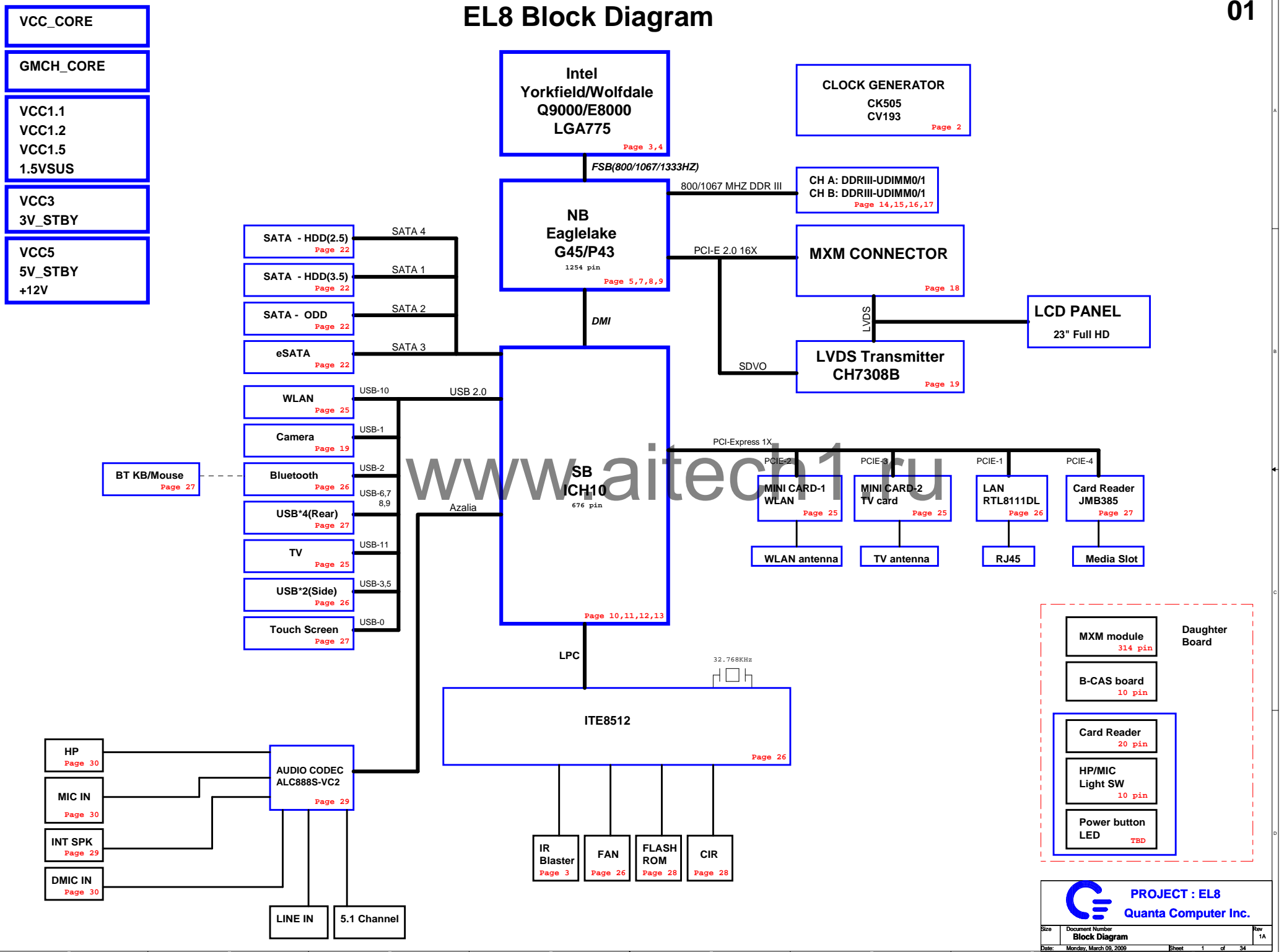
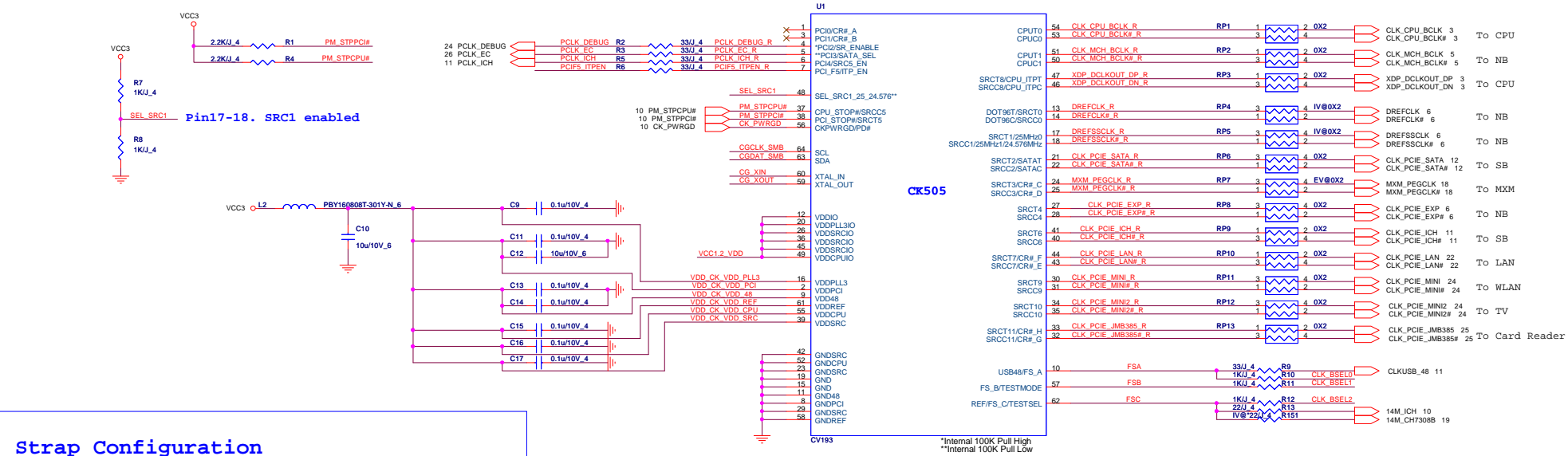


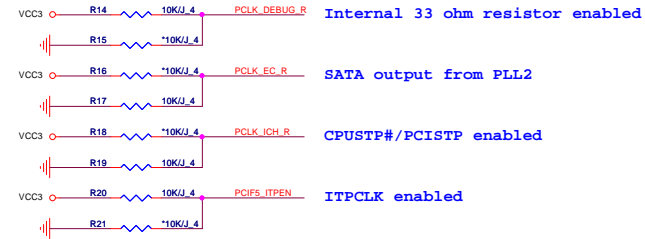
EL8 Block Diagram

01





Strap Configuration

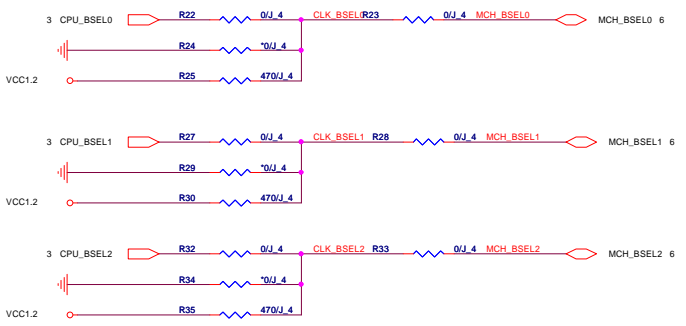


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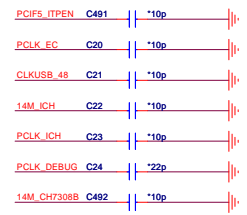
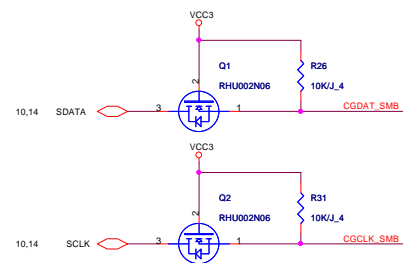
FREQ. SEL TABLE


BSEL Frequency Select Table

FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	0	0	333Mhz
1	0	1	100Mhz
1	1	0	400Mhz
1	1	1	Reserved



Clock Gen I2C

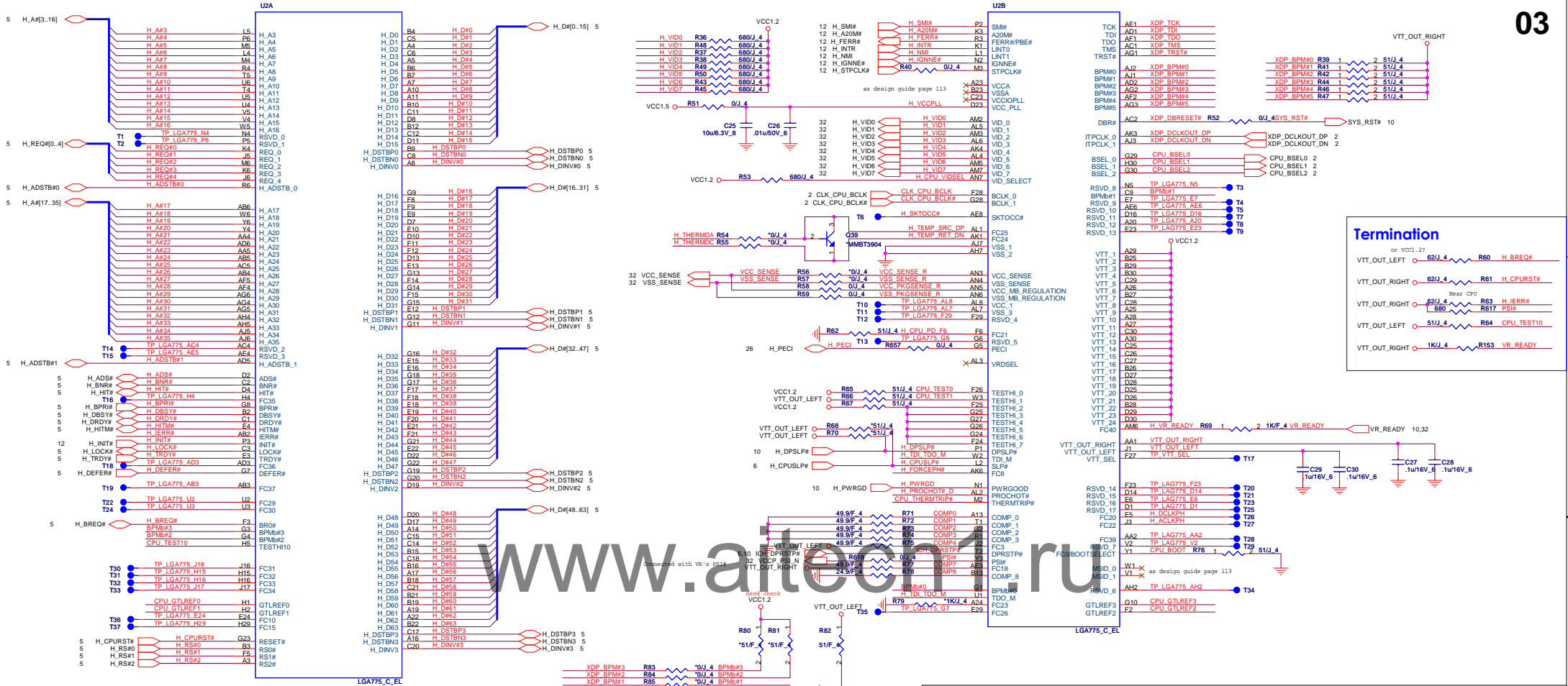


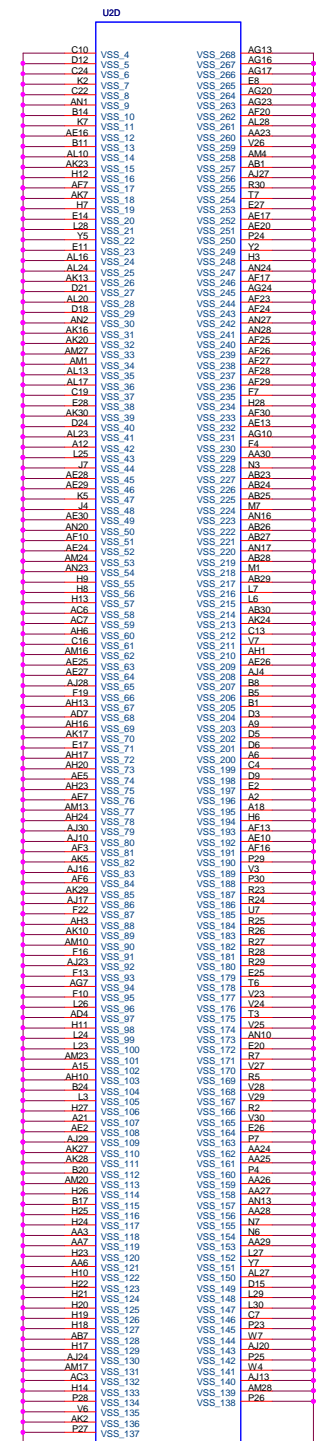


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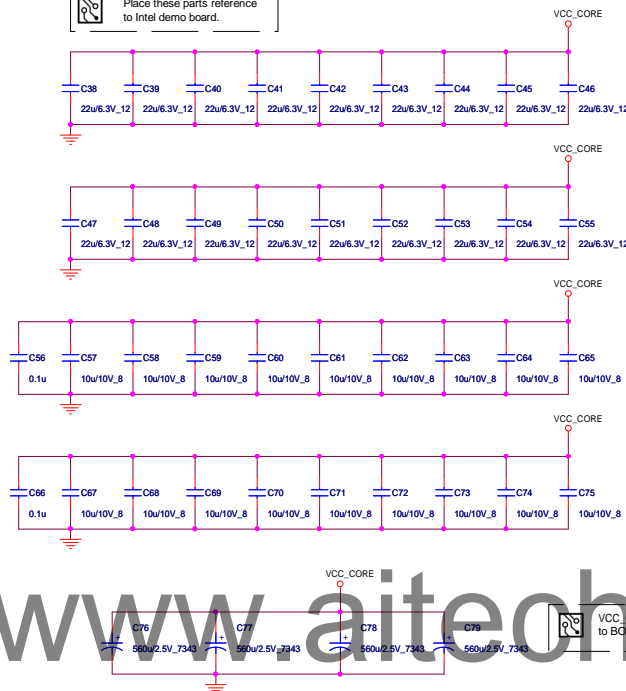
Size	Document Number	Rev
	CLK_GEN/CK505	1A

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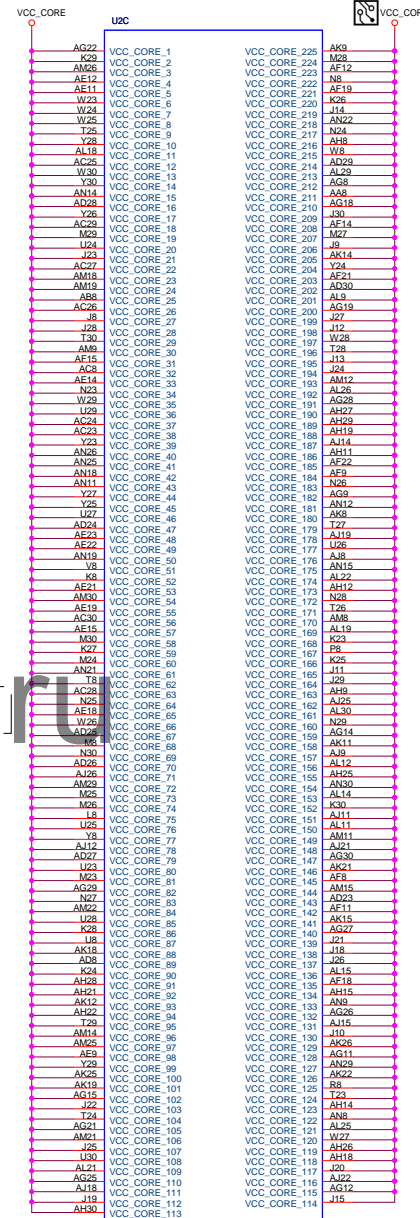
Place these parts reference to Intel demo board.

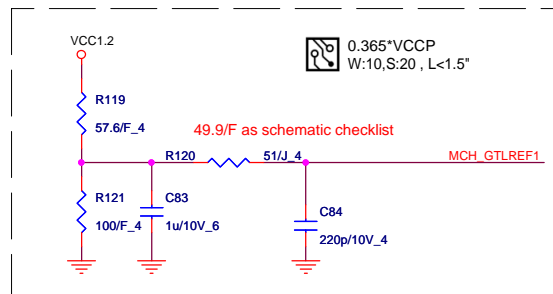


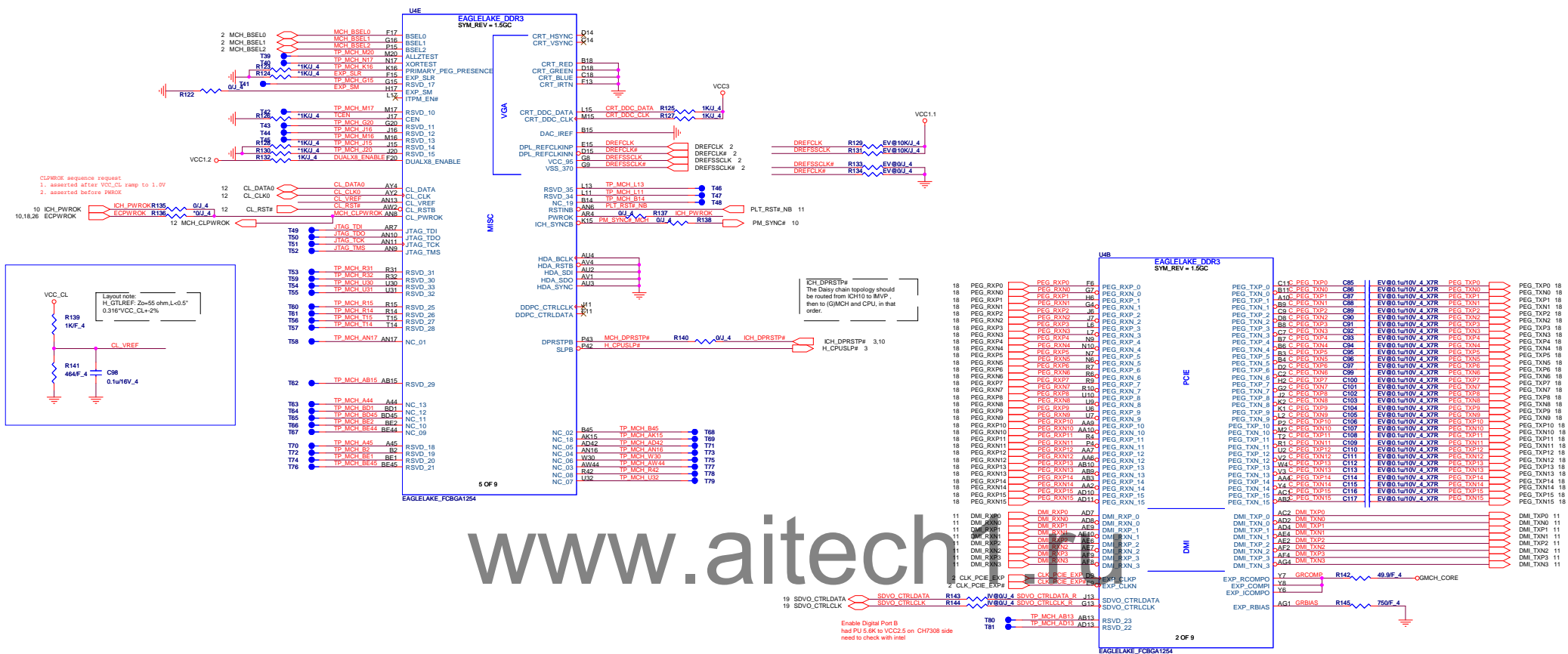
VCC_CORE Bulk CAPs place to BOT of CPU central

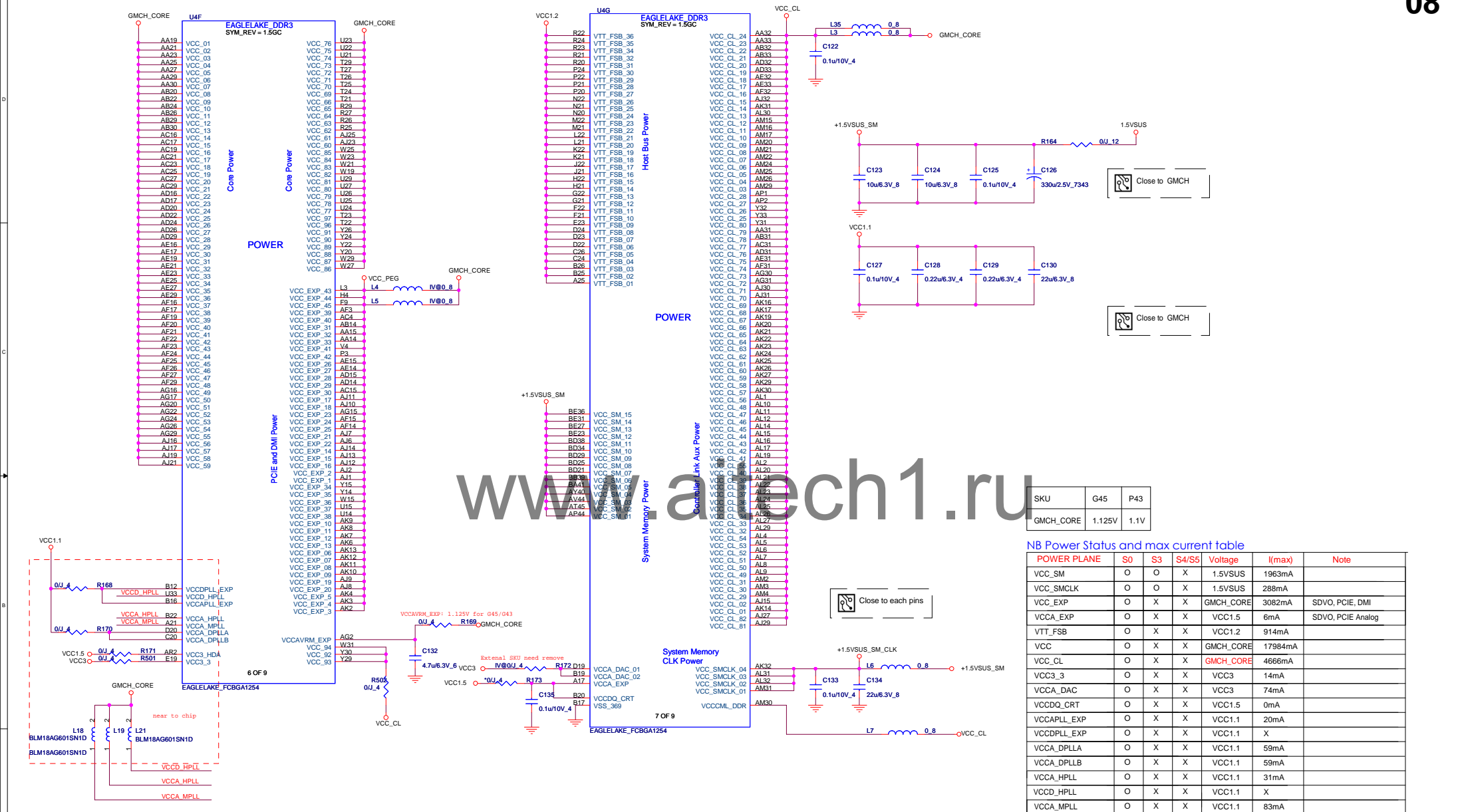
Yorkfield/Wolfdale CPU Power Status and max current table

POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC_CORE	O	X	X	VID	100A	Yorkfield@65W
VCC_CORE	O	X	X	VID	75A	Wolfdale
VTT	O	X	X	VCC1.2	8A	After VCC stable
VTT	O	X	X	VCC1.2	7A	Before VCC stable
VCC_PLL	O	X	X	VCC1.5	280mA	

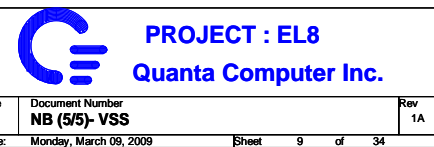




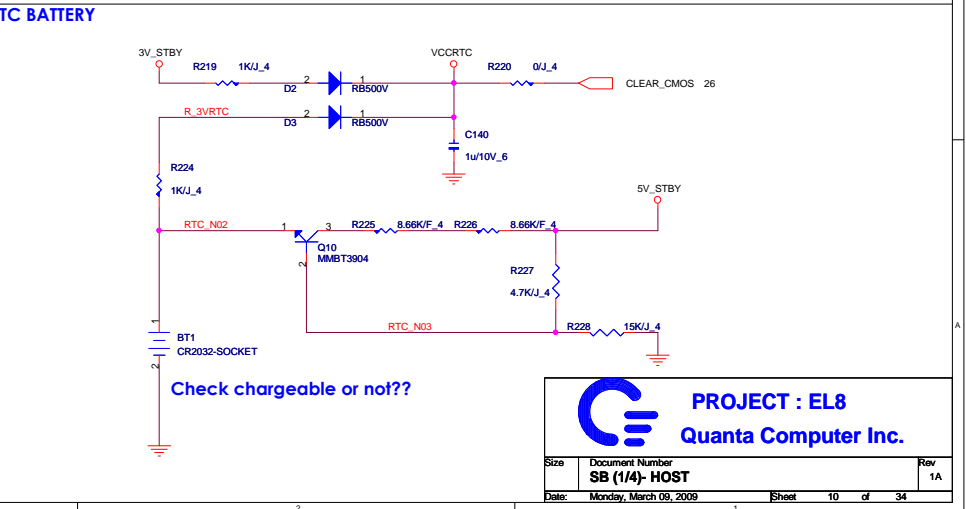
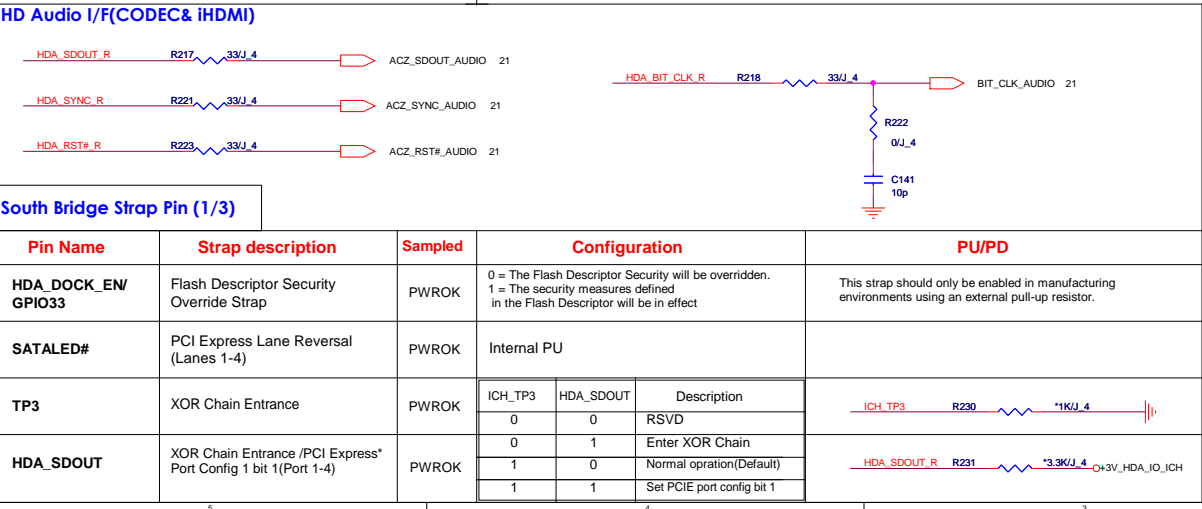
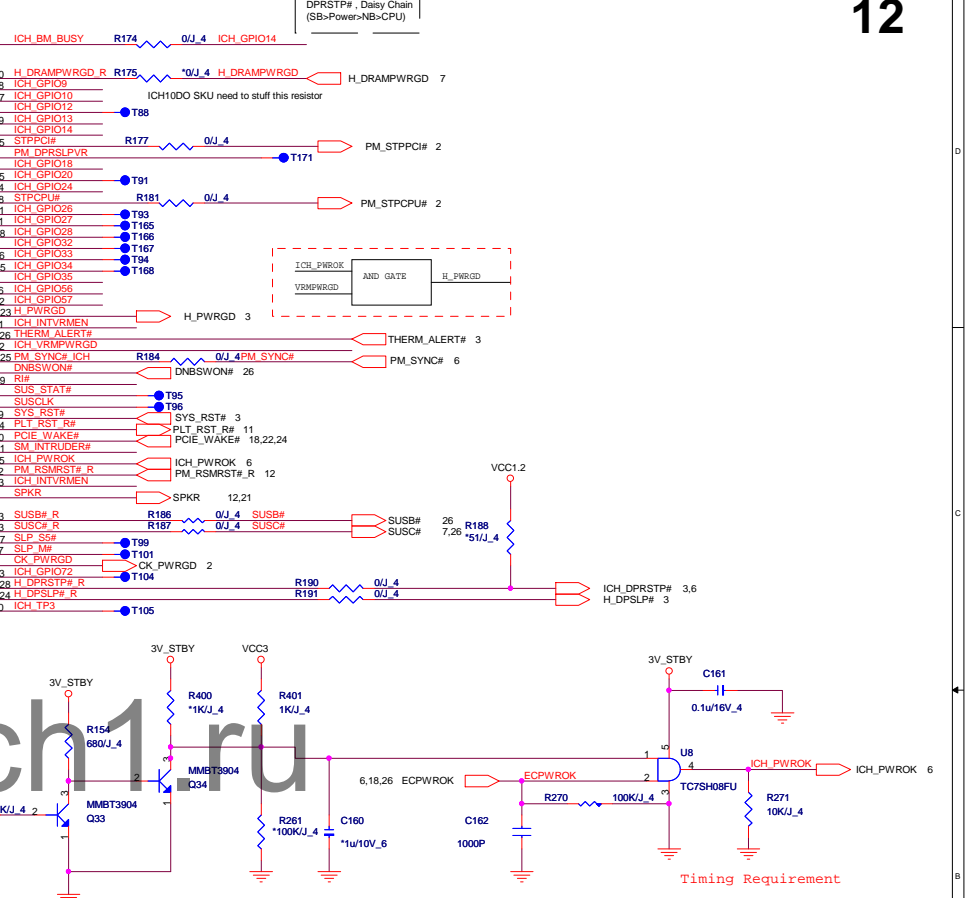
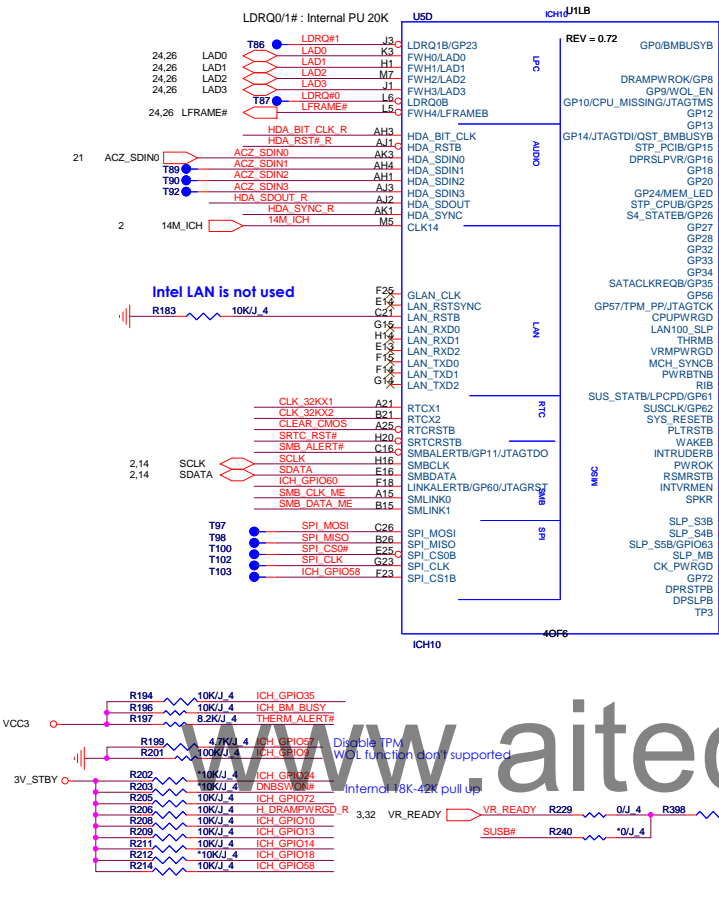
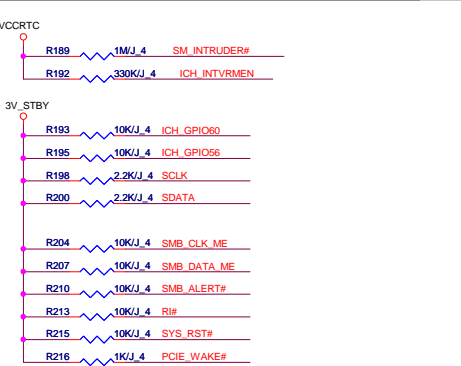


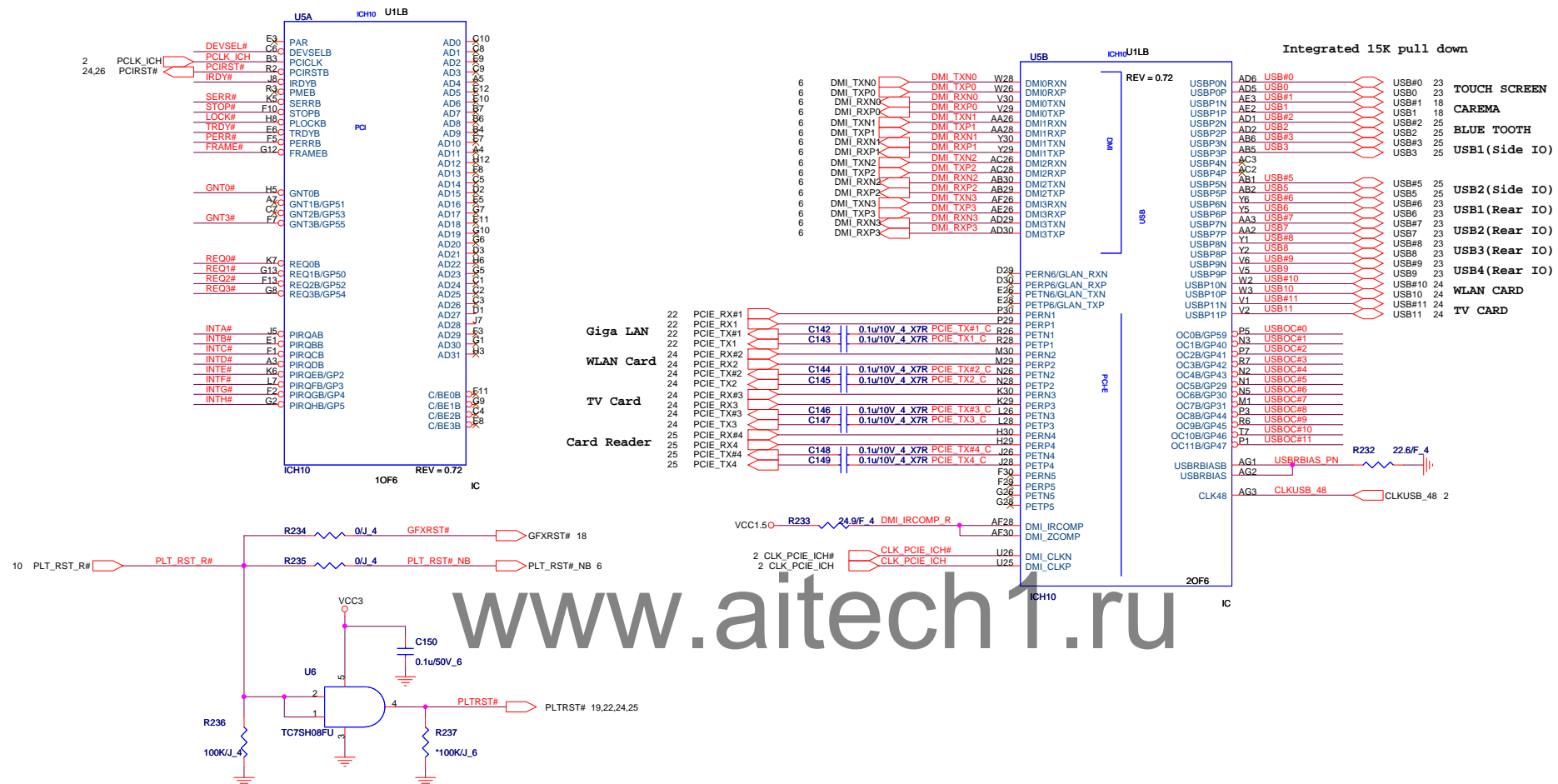


U4H
EAGLELAKE_FCBGA1254
SYM_REF = 1.5GC
8 OF 9





South Bridge Strap Pin (1/3)

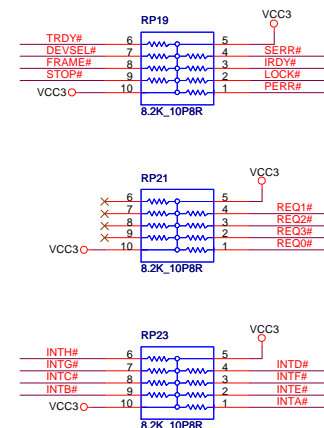




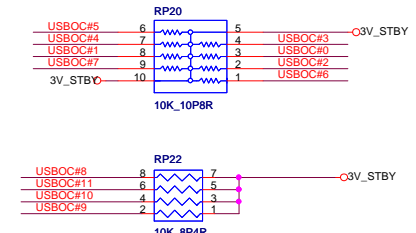
South Bridge Strap Pin (2/3)

Pin Name	Strap description	Sampled	Configuration			PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0			
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default			
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default			
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default			
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0	SPI_CS#1	Boot Location	
			0	1	SPI(Default)	
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1	0	PCI	
			1	1	LPC	

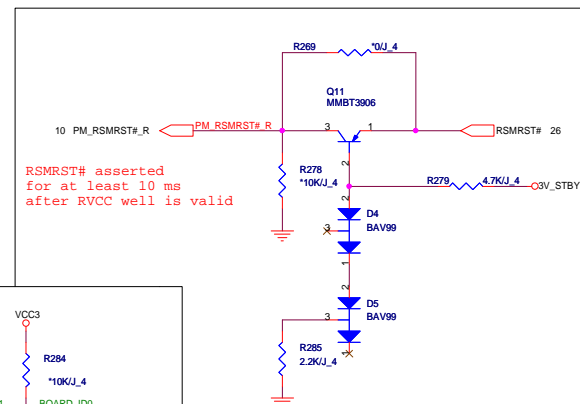
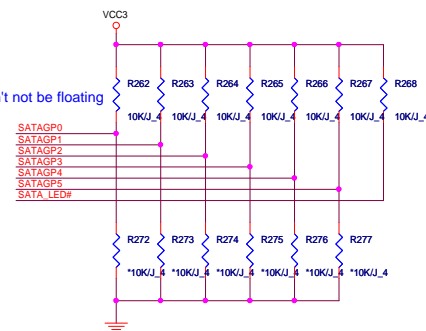
PCI PULL-UP



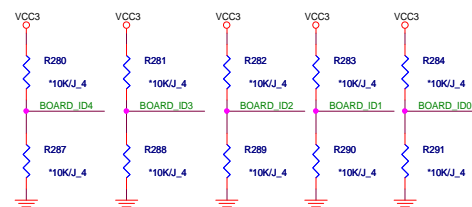
USBOC# PULL-UP

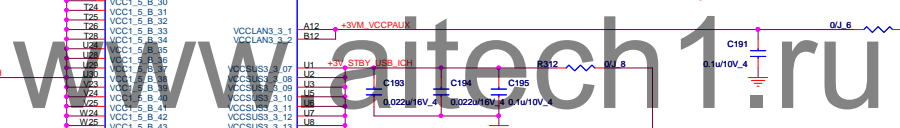


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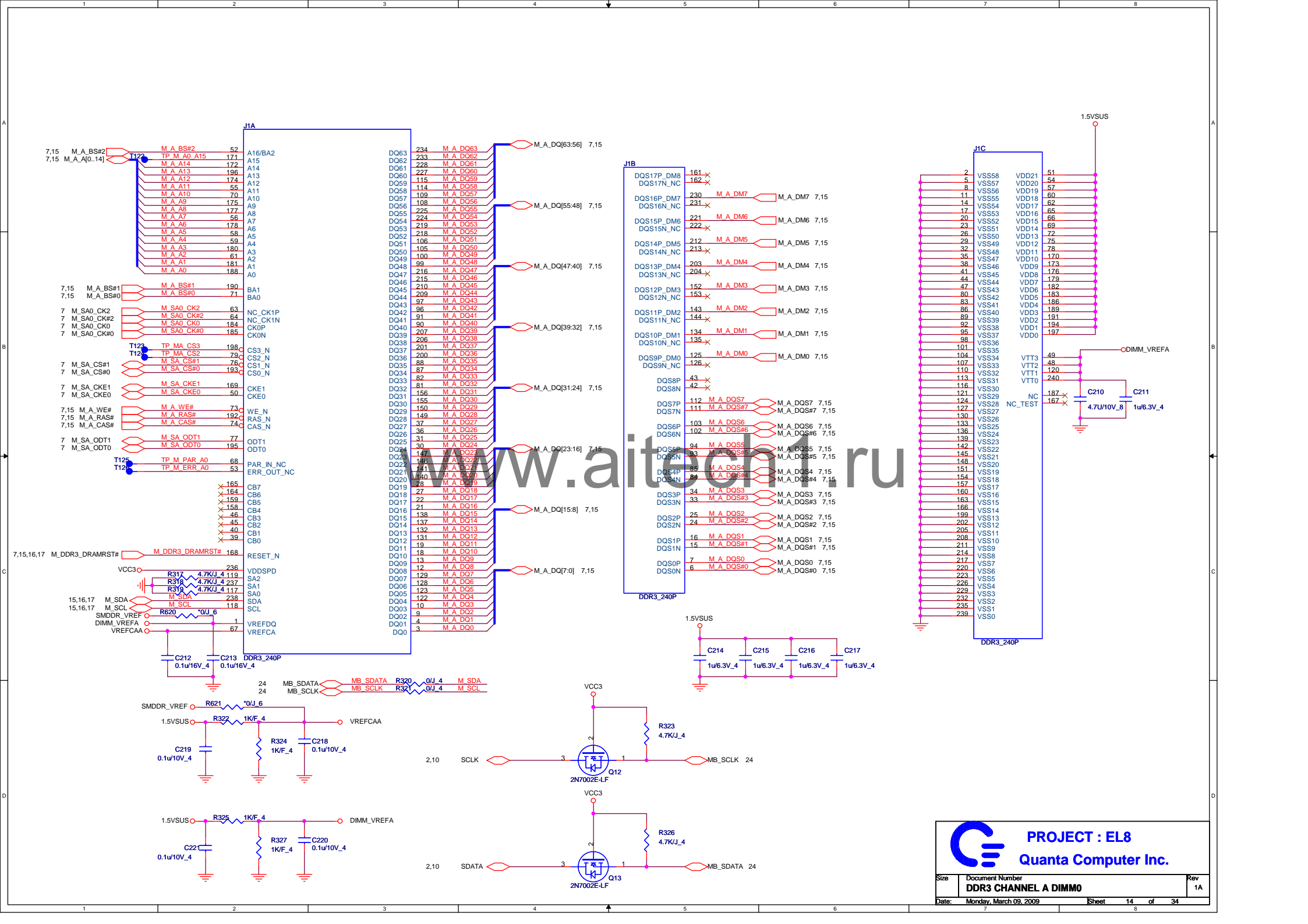
Board ID Table					
BOARD_ID3 of TE1M always keep low, TE1 hasn't support TV					
Board ID	ID4	ID3	ID2	ID1	ID0
NEW CARD CARD BUS					H L
CCFL Panel LED Panel				H L	
W/ G-SENSOR W/O G-SENSOR			H L		
W/ TV W/O TV		H L			
W/ HDMI W/O HDMI	H L				

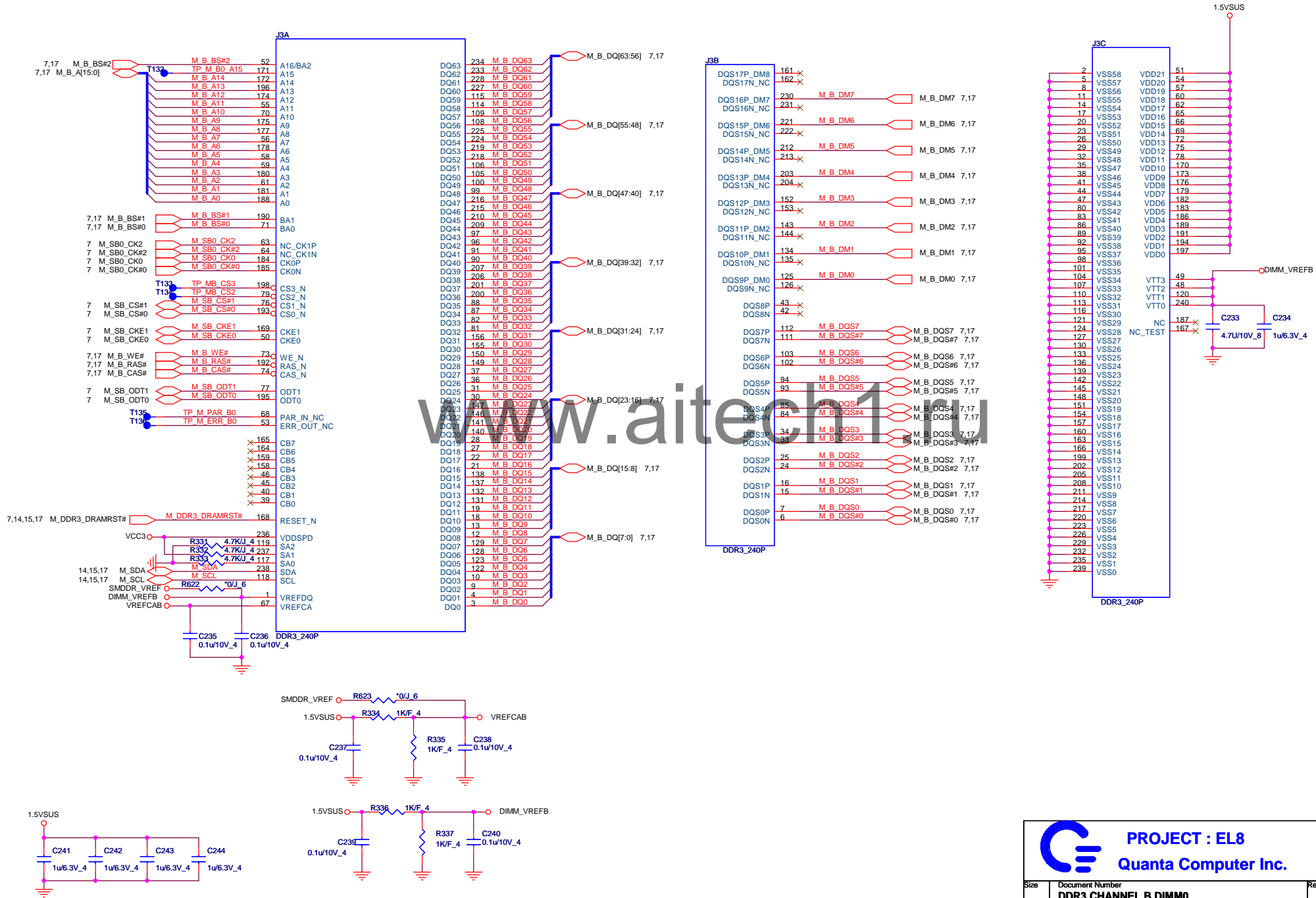


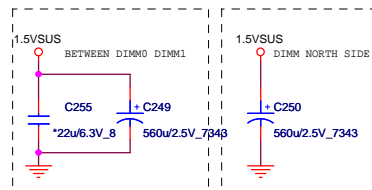


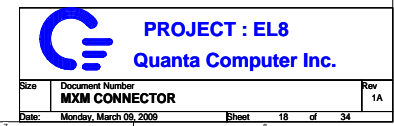
SB Power Status and max current table(2/2)

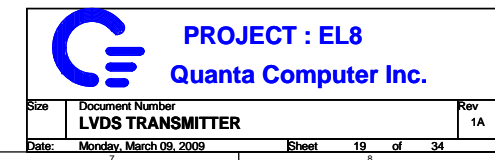
SB Power Status and max current table(2/2)						
POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC1_1	0	X	X	VCC1.1	1.634A	ICH CORE
VCCDMPILL	0	X	X	VCC1.5	23mA	
VCC_DMI	0	X	X	GMCH_CORE	50mA	1.125V@G45, 1.1V@P43
V_CPU_I/O	0	X	X	VCC1.2	2mA	
VCC3_3	0	X	X	VCC3	308mA	
VCC4DA	0	X	X	VCC1.5	70mA	
VCCSUSHD	0	0	0	RVCC1.5	70mA	
VCCSUS1_1	X	X	X	1.1V	X	Internal VR powered
VCCSUS1_5	X	X	X	1.5V	X	Internal VR powered
VCCSUS3_3	0	0	0	3V_STBY	212mA	53mA@S3/S5
VCCCL1_1	X	X	X	1.1V	X	Internal VR powered
VCCCL1_5	X	X	X	1.5V	X	Internal VR powered
VCCCL3_3	0	X	X	VCC3	73mA	S3/S5 powered when AMT active

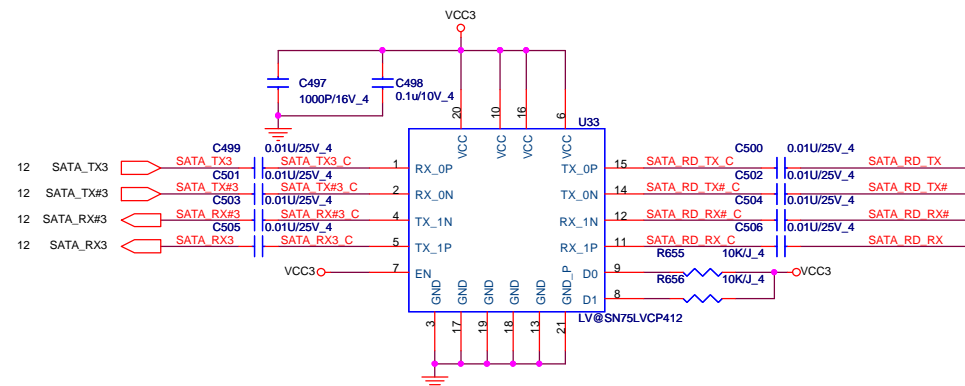
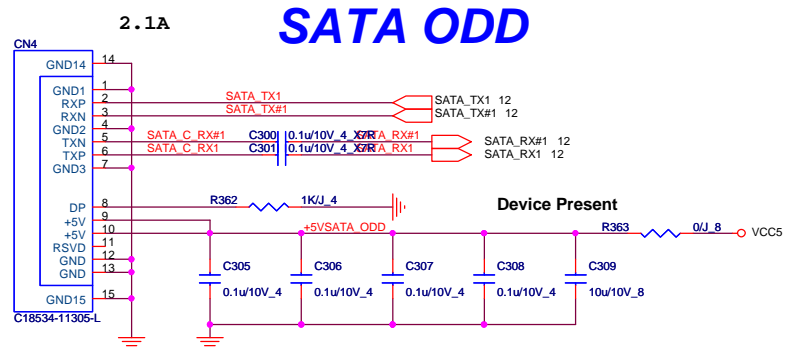






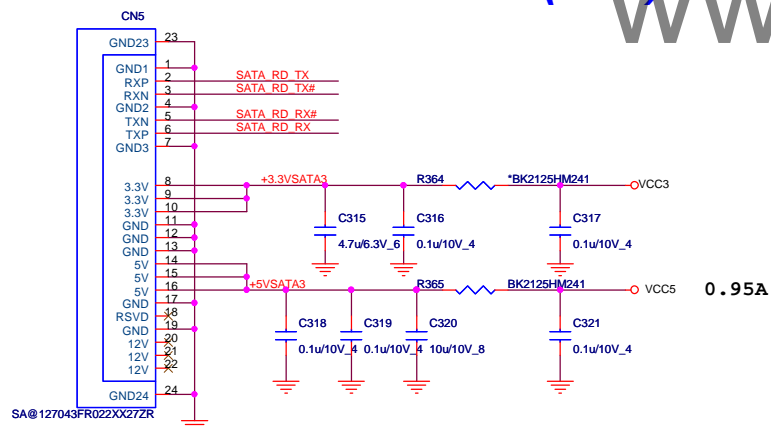




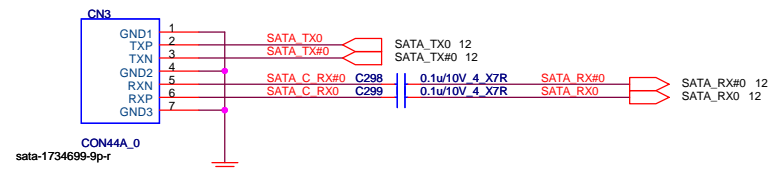


2nd SATA HDD(2.5")

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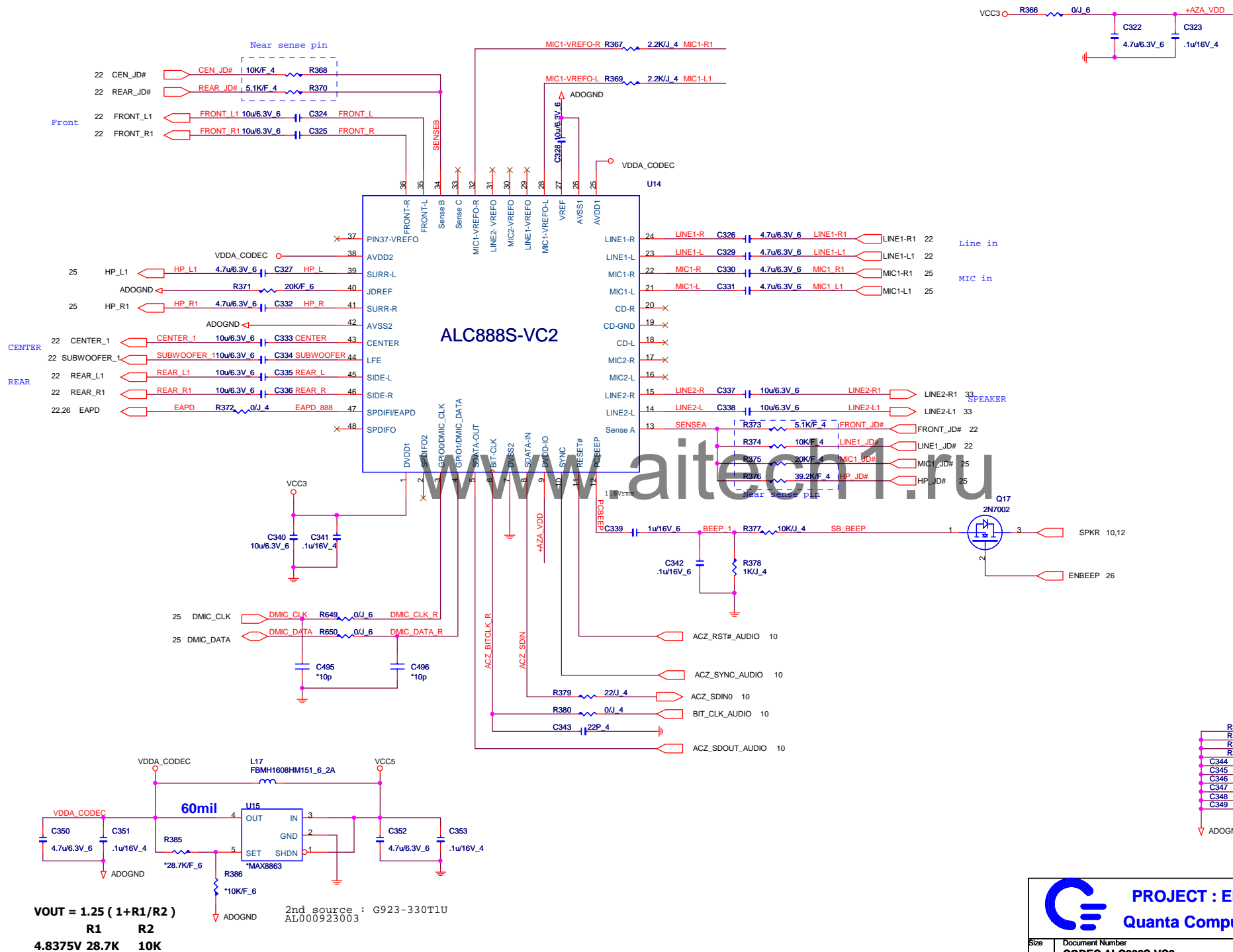


SATA HDD(3.5")



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CODEC



11 USB#6 USB#6



USBVCC4 : 40 mil



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CID: 050

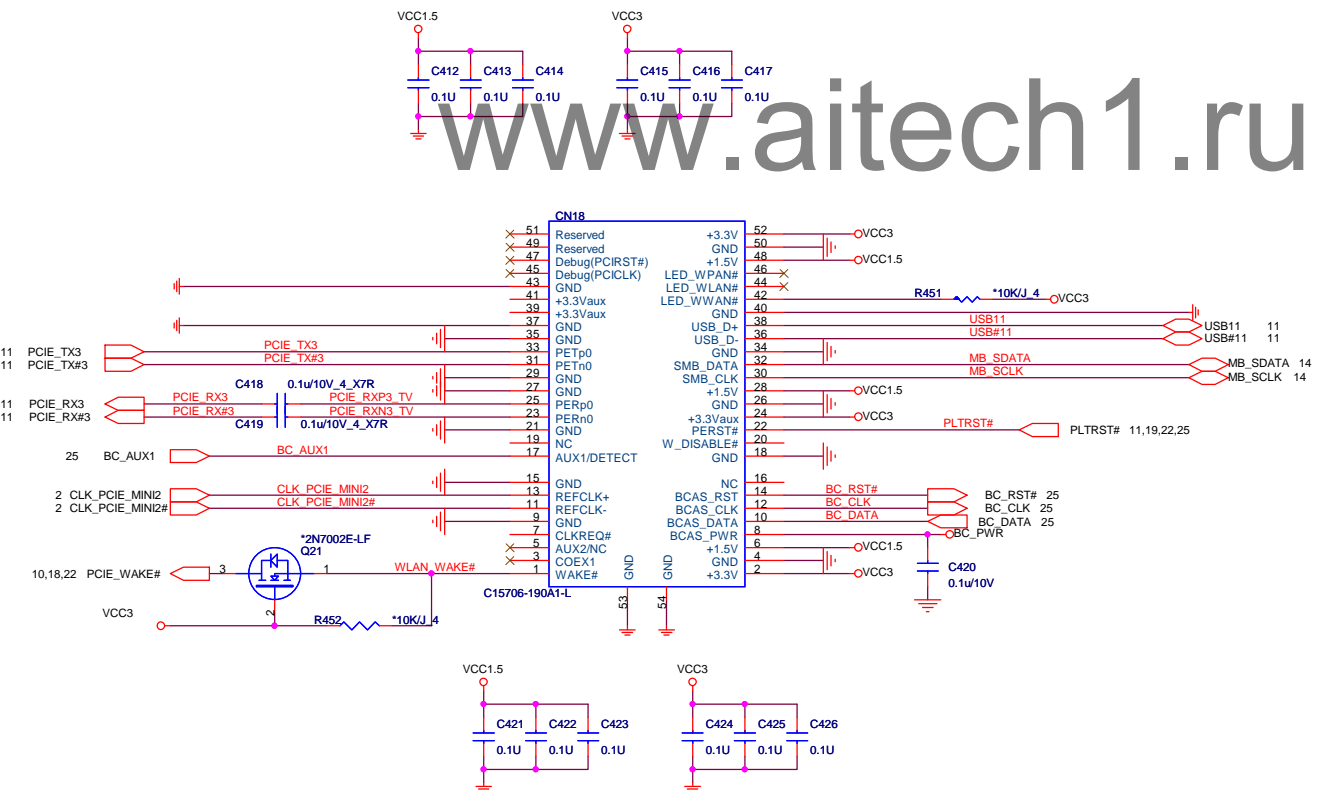
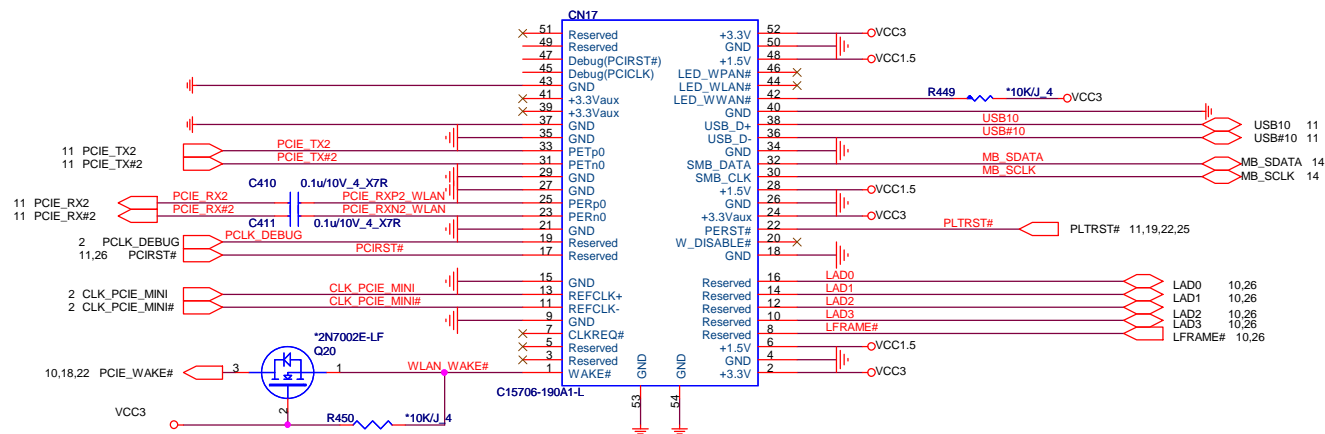
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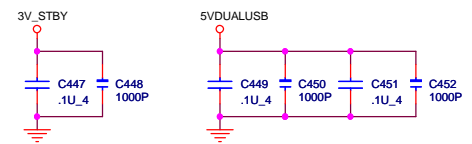
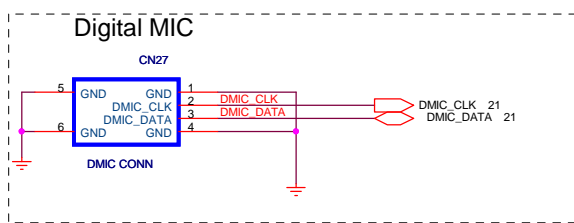
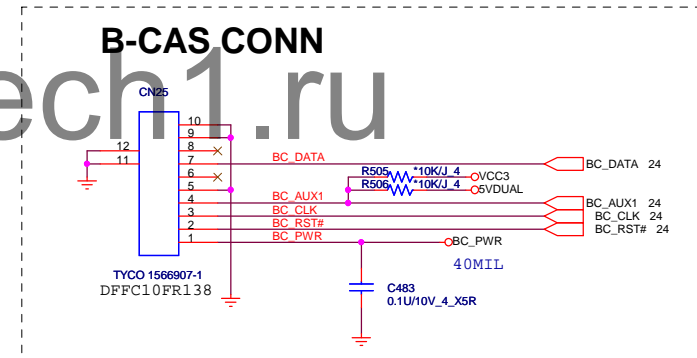
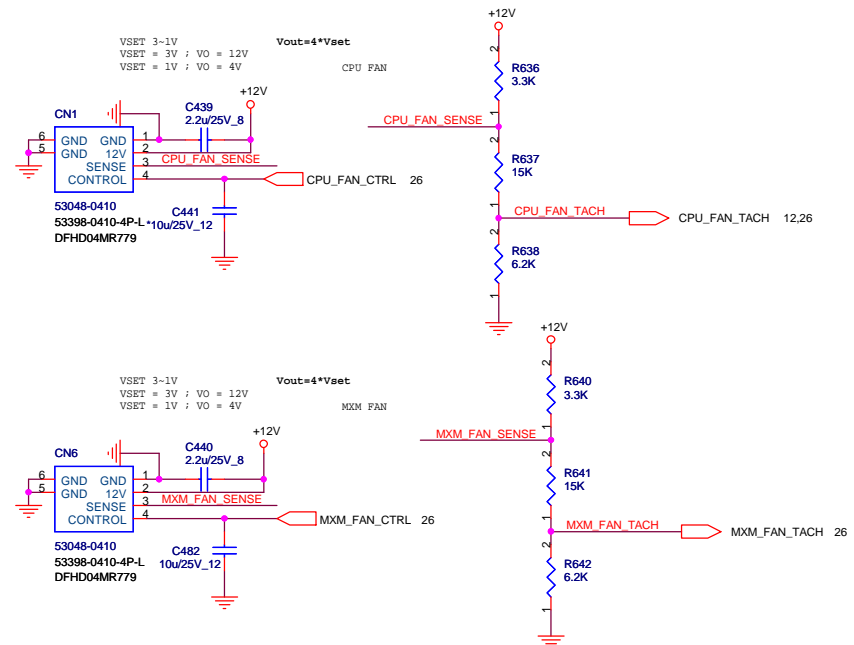
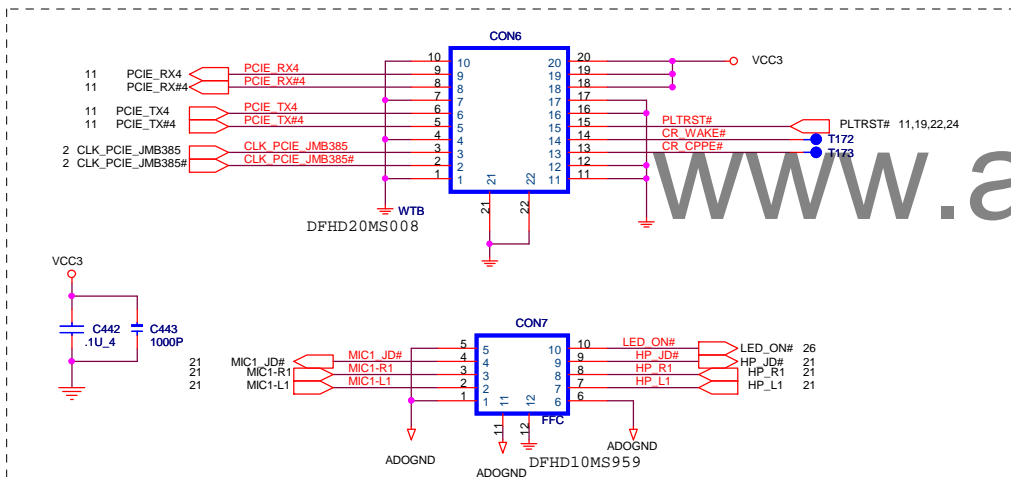
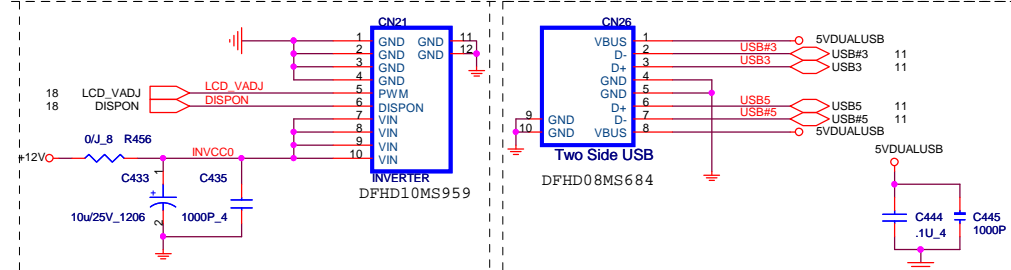
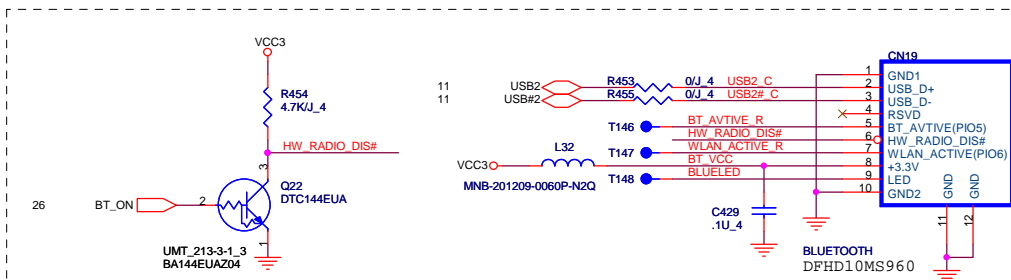
7

A horizontal number line with arrows at both ends. A pink dot is placed on the line, and the number 3 is written to its right.

85205-
DEVE



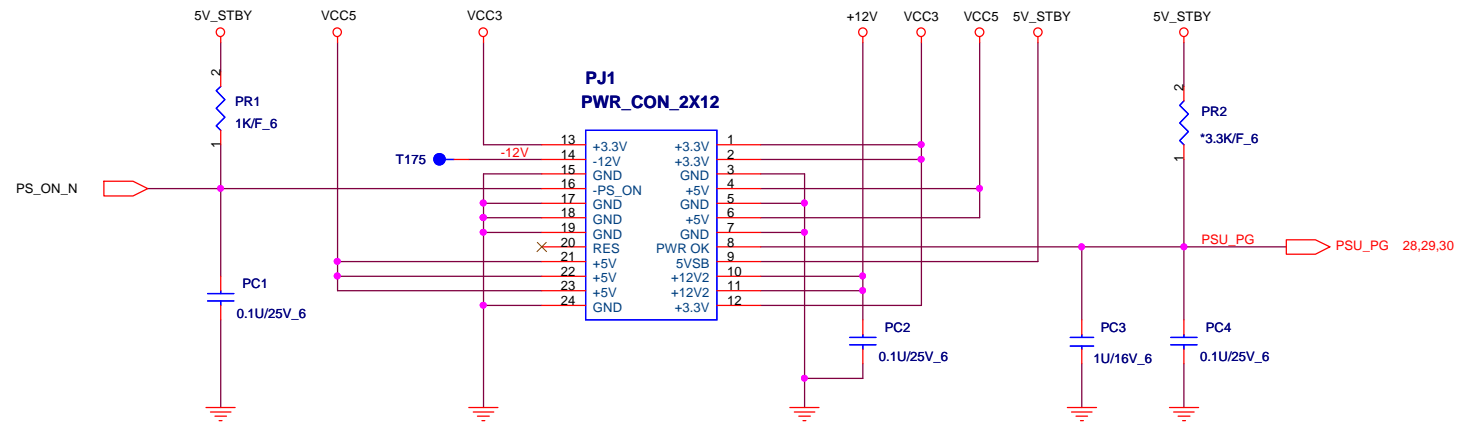




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Size: **CONNECTOR**
 Document Number: **CONNECTOR**
 Date: Monday, March 09, 2009
 Sheet: 25 of 34
 Rev: 1A

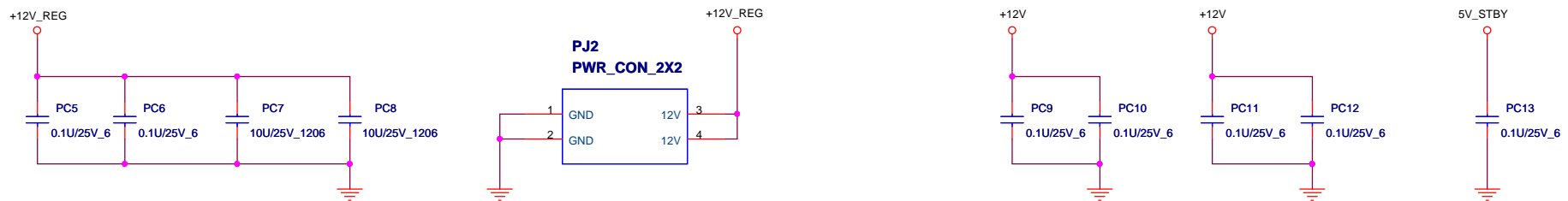
PSU 24PIN Connector



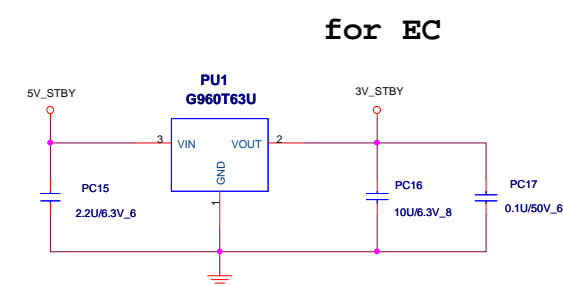
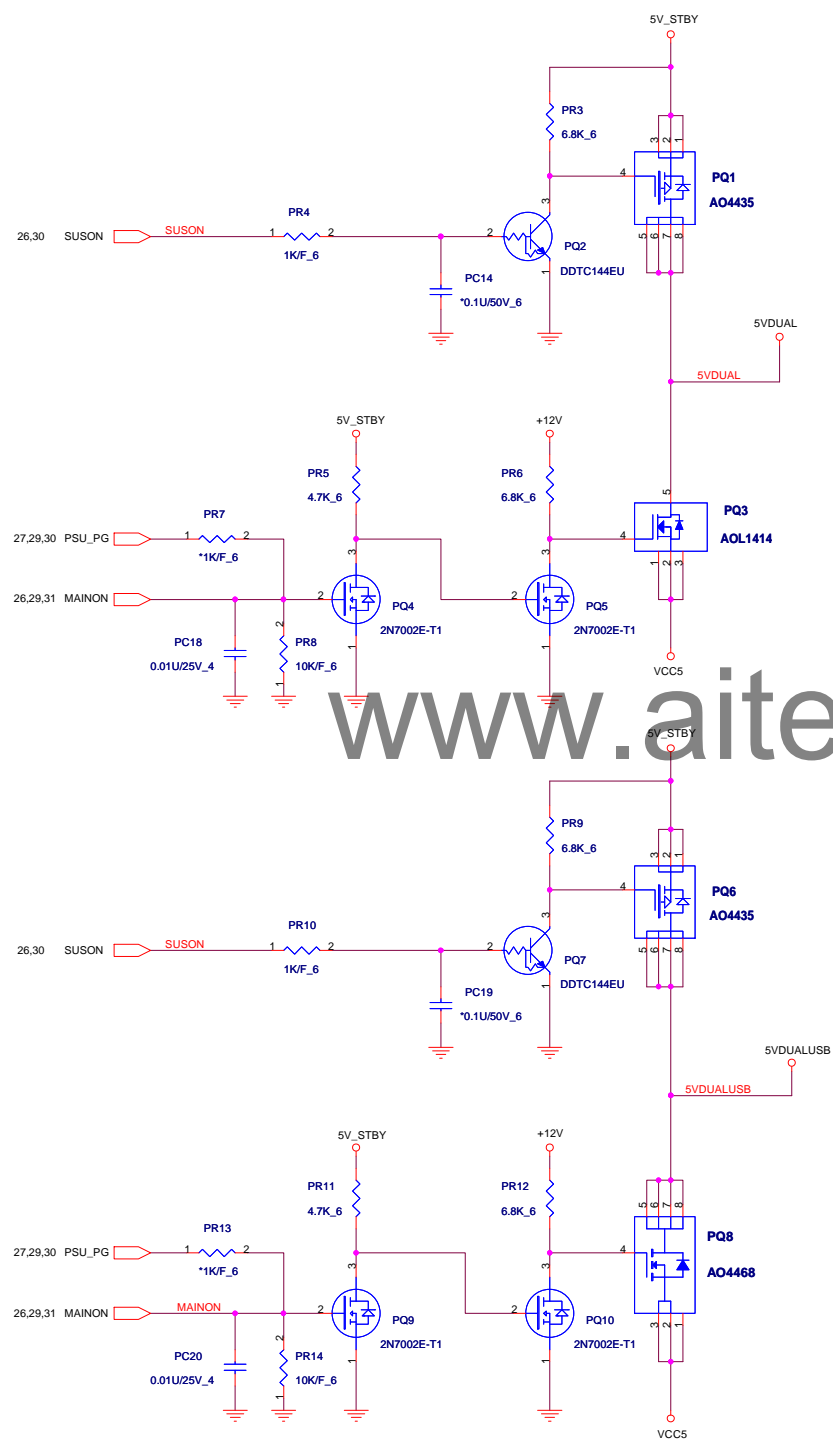
P3V3_STB : Stand-by power source only
 P3V3 : Normal power source only
 P3V3_DUAL : Both power source switching

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4PIN +12V_REG for CPU_CORE

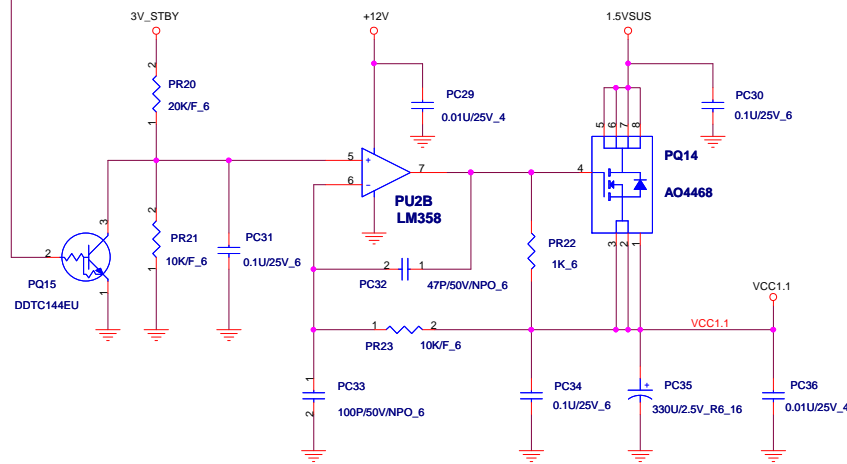
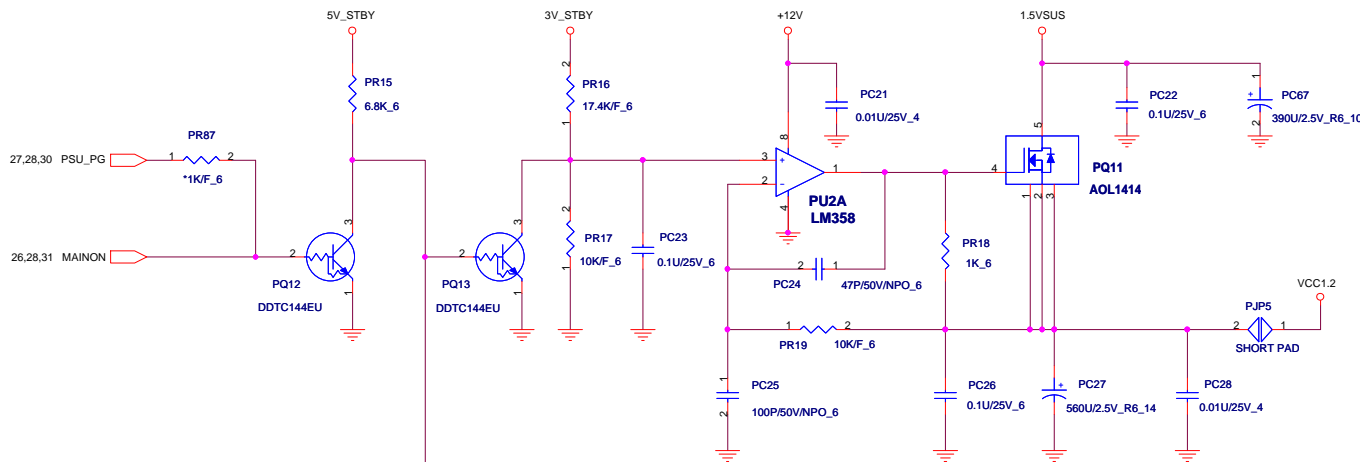


5VDUAL, 5VDUALUSB, 3V_STBY

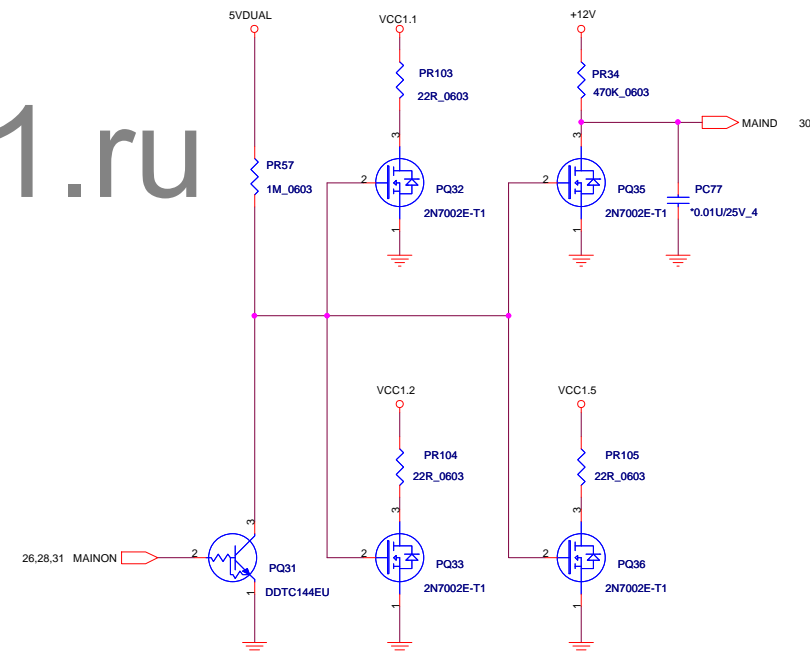


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VCC1.2, VCC1.1

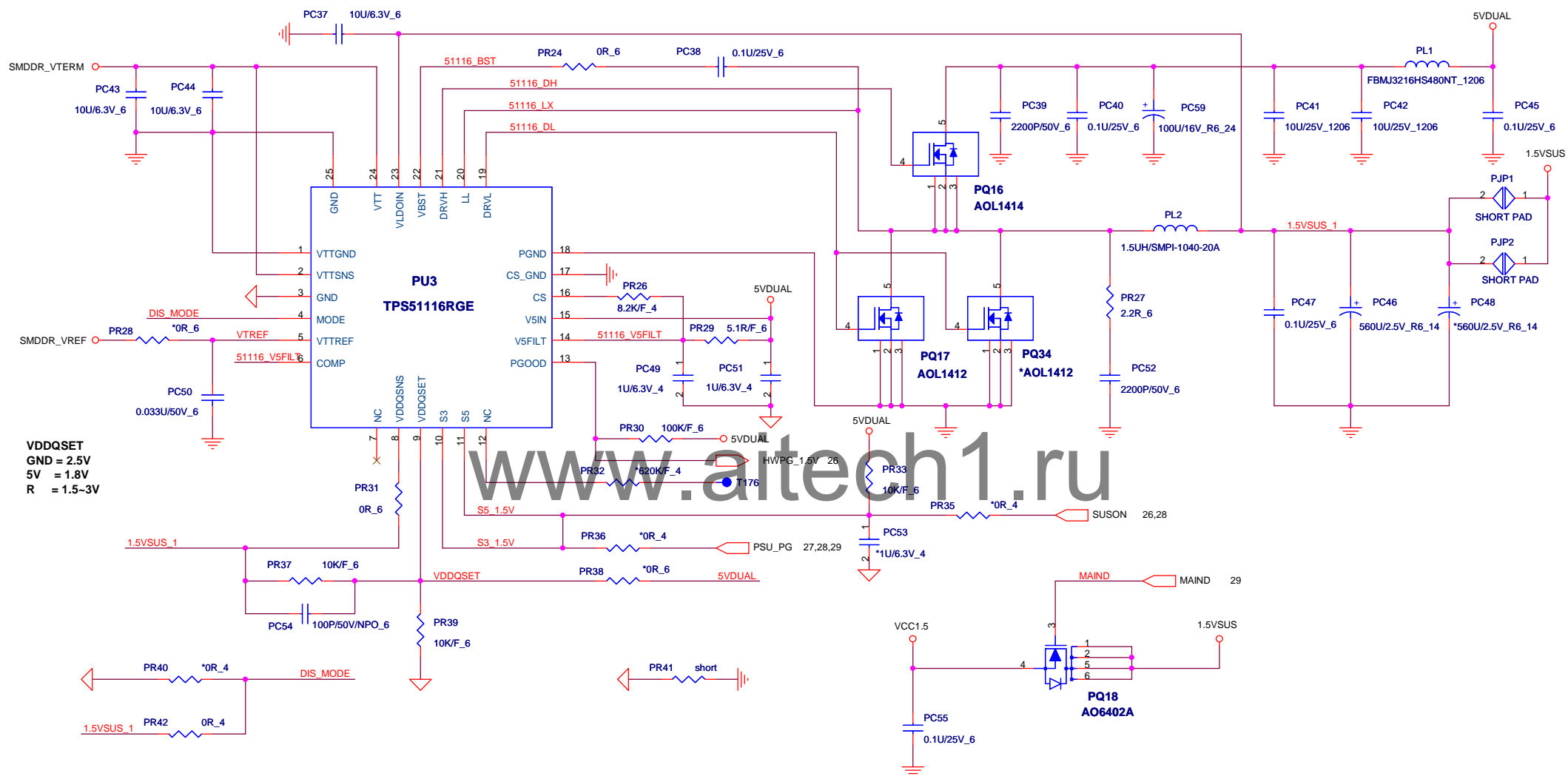


For ICH10



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DDR3 1.5V(TPS51116)

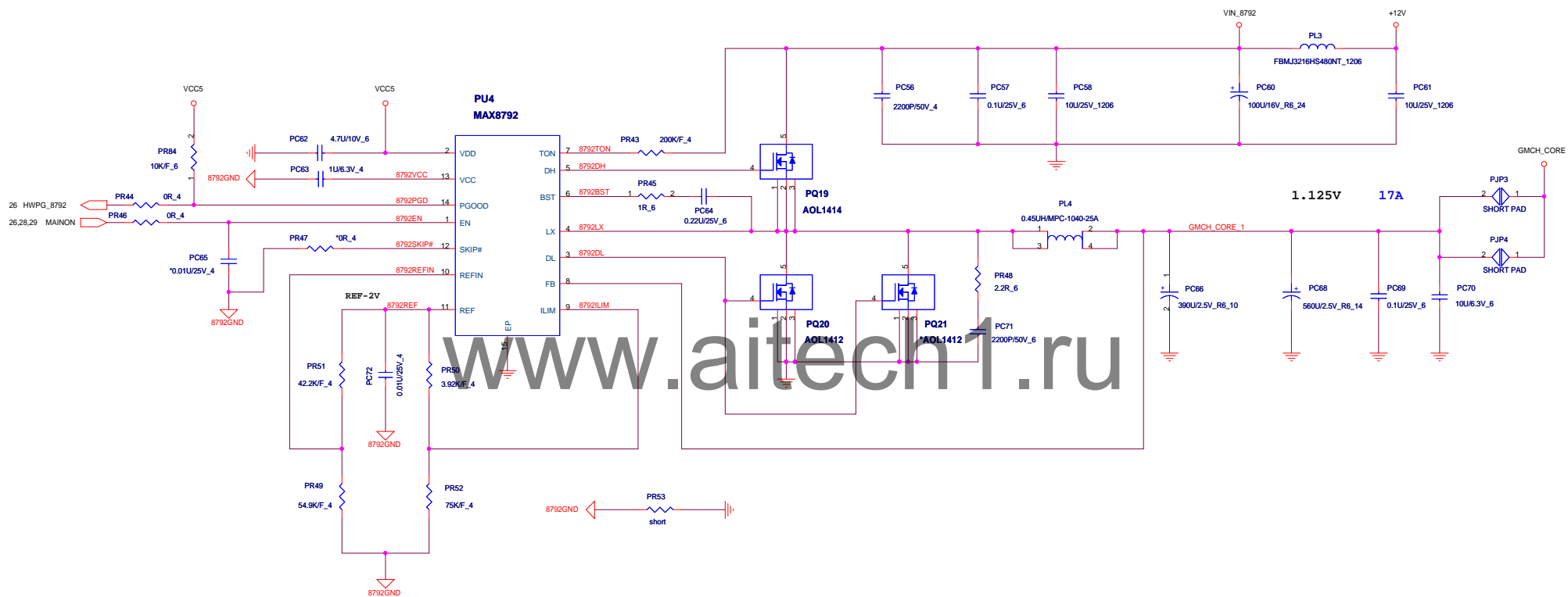


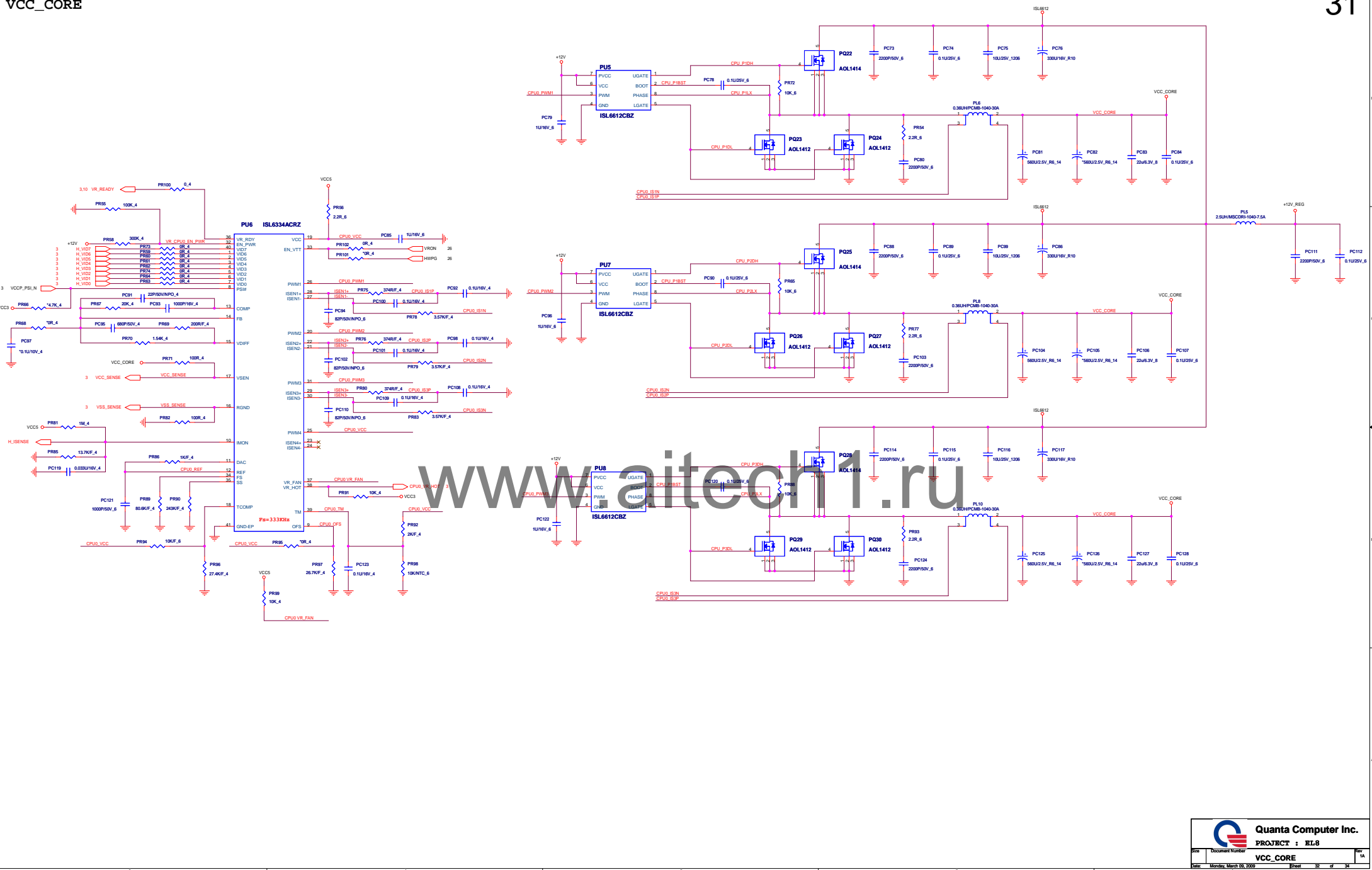
$$del_IL = (5V - 1.5V) \times 1.5V / (1.5\mu \times 400K \times 19V) = 4.6A$$

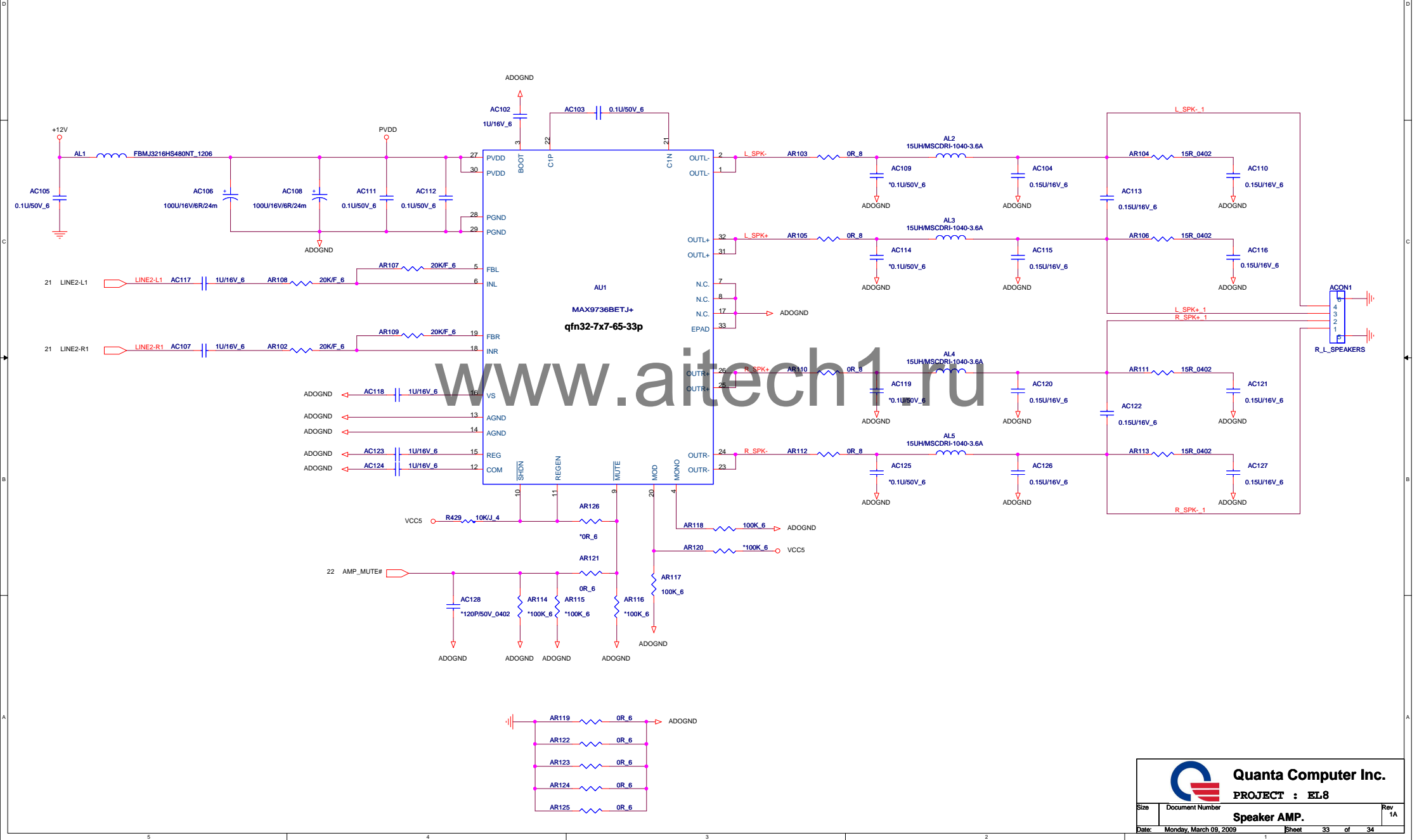
$$(10\mu A \times PR26 / R_{dson}) + del_IL / 2 = I_{ocp}$$

$$(10\mu A \times 8.2K / 4.6m) + del_IL / 2 = 20.1A$$

G43 GMCH_CORE







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